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APPLICATION NO. **FILING DATE** FIRST NAMED INVENTOR ATTORNEY DOCKET NO. 5 5181-15900/P 06/15/98 HANSON 09/097,468 **EXAMINER** LM02/0607 ELISCA, P B NOEL KIVLIN CONLEY ROSE & TAYON **ART UNIT** PAPER NUMBER P 0 BOX 398 2785 AUSTIN TX 78701-0398

Please find below and/or attached an Office communication concerning this application or proceeding.

Commissioner of Patents and Trademarks

06/07/00

Office Action Summary

Application No. 09/097,468

Applicant(s)

Hanson et al.

Examiner

Pierre Eddy Elisca

Group Art Unit

2785



X Responsive to communication(s) filed on Jun 15, 1998	·
☐ This action is FINAL .	
☐ Since this application is in condition for allowance except fo in accordance with the practice under <i>Ex parte Quayle</i> , 193	
A shortened statutory period for response to this action is set to is longer, from the mailing date of this communication. Failure application to become abandoned. (35 U.S.C. § 133). Extensi 37 CFR 1.136(a).	to respond within the period for response will cause the
Disposition of Claims	
	is/are pending in the application.
Of the above, claim(s) none	is/are withdrawn from consideration.
Claim(s)	is/are allowed.
Claim(s)	
☐ Claims	
Application Papers	
☒ See the attached Notice of Draftsperson's Patent Drawing	g Review, PTO-948.
☐ The drawing(s) filed on is/are object	ted to by the Examiner.
☐ The proposed drawing correction, filed on	is 🗔 pproved 🖂 disapproved.
☐ The specification is objected to by the Examiner.	
\square The oath or declaration is objected to by the Examiner.	
Priority under 35 U.S.C. § 119	
☐ Acknowledgement is made of a claim for foreign priority	under 35 U.S.C. § 119(a)-(d).
☐ All ☐ Some* ☐ None of the CERTIFIED copies of	f the priority documents have been
received.	
☐ received in Application No. (Series Code/Serial Nur	nber)
received in this national stage application from the	
*Certified copies not received:	
Acknowledgement is made of a claim for domestic priorit	ty under 35 U.S.C. § 119(e).
Attachment(s)	
Notice of References Cited, PTO-892 .	
☑ Information Disclosure Statement(s), PTO-1449, Paper No.	o(s). <u>4 and 5</u>
☐ Interview Summary, PTO-413	-
Notice of Draftsperson's Patent Drawing Review, PTO-94	18
☐ Notice of Informal Patent Application, PTO-152	
SEE OFFICE ACTION ON 1	THE FOLLOWING PAGES
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Examiner Pierre Eddy Elisca

United States Department of Commerce

Patent and Trademark Office

Washington, D. C. 20231

DETAILED ACTION

1. This office action is in response to application serial number 09/097,468, filed on 06/15/1998.

Claim Rejections - 35 USC § 103

- 2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:
 - (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.
- 3. Claims 1-26, are rejected under 35 U.S.C. 103 (a) as being unpatentable over Tavallaei et al. (U.S. pat. No. 5,864,653) in view of Splett et al. (U.S. Pat. No. 5,001,712).

As per claims 1, 6, 7, 8, 10-20, 23-26, Tavallaei substantially discloses a PCI hot spare capability for failed components and a SMC for running boundary scan test on the system which is

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equivalent to the test mechanism for testing device driver see., applicant fig 1 and Tavallaei figs 1 and 2, col 4, lines 1-12, lines 38-63, col 7, lines 3-56. Not specifically disclose by **Tavallaei et al.** is the step of intercepting the device access call from a device driver under test and faults to be injected in response to the device driver(or computer program). However, **Splett et al.** discloses a diagnostic error injection and software programs for a bus system wherein valid bus signal lines are intercepted in order to inject error within the system.

Tavallaei and Splett are analogous art because they are from the similar problem solving area of testing peripheral devices.

At the time of the invention it would have been obvious to a person of ordinary skill in the art to combine the PCI hot spare capability for failed components of **Tavallaei et al.** with the software injection of **Splett et al.** because such combination would allow the PCI hot spare capability for failed components to specify exactly when the error will occur on the bus and to program any error or combination of errors during a bus cycle (see., Splett, col 2, lines 51-54).

As per claims 2, 3, 4, 9, 21, 22, Splett discloses the claimed limitation wherein the intercept mechanism comprises a plurality of intercept routines (see., col 2, lines 36-54).

As per claim 5, Tavallaei discloses the claimed limitation wherein the mapping mechanism comprises a look-up table (see., col 15, lines 44-67, col 16, lines 34-58).

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Conclusion

4. The prior art made of record and relied upon is considered to applicant's disclosure.

5. Any inquiry concerning this communication from the examiner should be directed to Pierre Eddy Elisca at (703) 305-3987. The examiner can normally be reached on Tuesday to Friday from 6:30AM. to 5:00PM.

If any attempt to reach the examiner by telephone is unsuccessful, the examiner's supervisor, Robert W. Beausoleil Jr can be reached on (703) 305-9713.

Any response to this action should be mailed to:

Commissioner of patents and Trademarks

Washington, D.C. 20231

or faxed to:

(703) 308-9051, (for formal communications intended for entry)

OR:

(703) 305-3718 (for informal or draft communications, pleased label

"PROPOSED" or" DRAFT")

Hand-delivered responses should be brought to Crystal Park II, 2121 Crystal Drive, Arlington.

VA., Sixth floor (receptionist).

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Patent Examiner

June 2, 2000

HOBER! W. BEAUSOLIEL, JR. SUPERVISORY PATENT EXAMINER GROUP 2700